integrators;

a chip-sequence decoder, coupled to said comparator, for decoding the largest value from a respective integrator of said plurality of integrators, into N bits of interleaved data;

a deinterleaver, coupled to said chip-sequence decoder, for deinterleaving a series of interleaved bits from said chip-sequence decoder, as deinterleaved data; and

a FEC decoder, coupled to said deinterleaver, for FEC decoding the deinterleaved data as estimated data.

Claims 2-4 (cancel).

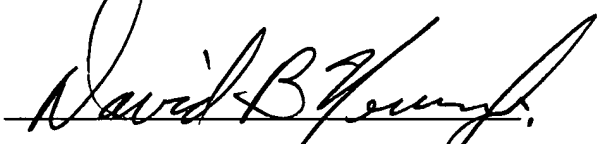
REMARKS

By this amendment, applicant cancels claims 2-4. Claim 1 is pending in the patent application.

Applicant also amends the Abstract.

Respectfully submitted,

DAVID NEWMAN CHARTERED

By: 

Date: October 6, 2003

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